This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-18(canceled).

19(new). A logic analyzer data retrieving method used in a logic analyzer comprising a control unit and a time delay circuit, wherein said control circuit comprises a memory and a second counter, and said time delay circuit comprises a first counter and a buffer, the method comprising the steps of:

providing and storing a time delay default value in said buffer of said time delay circuit;

presetting at least a clock qualifier signal based on a specific parameter;

triggering a preset of said first counter and transferring said default value from said buffer to said first counter to drive said first counter to start counting in response to said clock qualifier signal until said delay default value is reached;

capturing test data from a test sample electrically connected to the logic analyzer in response to said triggering of said preset of said first counter until said first counter counting reaches said delay default value, wherein said control unit is adopted for capturing said test data from a test sample; and

triggering a preset of said second counter, in response to said first counter counting reaching said delay default value, to start counting until the preset of the first counter is triggered again.

20(new). The logic analyzer data retrieving method as claimed in claim 19, wherein counting value of said second counter is stored in said memory unit when said second counter stops countng and then displaying the value on a display screen.

21(new). The logic analyzer data retrieving method as claimed in claim 19, further comprising a step of sampling clock input only during the period of a clock enable signal.

22(new). The logic analyzer data retrieving method as claimed in claim 21, wherein an output of said clock enable signal is low when said first counter starts counting, and the output of said clock enable signal is high when said first counter counted until said default value is reached.

23(new). A logic analyzer data retrieving method used in a logic analyzer comprising a control unit and a time delay circuit, wherein said control circuit comprises a memory and a second counter, and said time delay circuit comprises a first counter and a buffer, the method comprising the steps of:

providing and storing a time delay default value in said buffer of said time delay circuit;

presetting at least a clock qualifier signal based on a specific parameter;

triggering a preset of said first counter and transferring said default value from said buffer to said first counter to drive said first counter to start counting in response to said clock qualifier signal until said delay default value is reached;

capturing test data from a test sample electrically connected to the logic analyzer in response to said triggering of said preset of said first counter until said first counter counting reaches said delay default value, wherein said control unit is adopted for capturing said test data from a test sample; and

triggering a present of said second counter, in response to said first counter counting reaching said delay default value, to start counting until the preset of the first counter is triggered again, and wherein counting value of said second counter is stored in said memory unit when said second counter stops counting and then displaying the value on a display screen.

24(new). The logic analyzer data retrieving method as claimed in claim 23, further comprising a step of sampling clock input only during the period of a clock enable signal.

25(new). The logic analyzer data retrieving method as claimed in claim 24, wherein an output of said clock enable signal is low when said first counter starts counting, and the output of said clock enable signal is high when said first counter counted until said default value is reached.

26(new). A logic analyzer data retrieving circuit, comprising:

a control unit, comprising a memory and a second counter, adopted for capturing test data from a test sample electrically connected to the logic analyzer data retrieving circuit; and

a time delay circuit, comprising a first counter and a buffer, wherein said buffer is adopted for storing a time delay default value;

wherein at least a clock qualifier signal is preset in said logic analyzer data retrieving circuit based on a specific parameter,

wherein a preset of said first counter is triggered and said default value is transferred from said buffer to said first counter to drive said first counter to start counting in response to said clock qualifier signal until said delay default value is reached and test data from said test sample is continuously captured until said first counter counting reaches said delay default value, and

wherein a preset of said second counter is triggered when said first counter counting reaches said delay default value and starts counting until the present of the first counter is triggered again.

27(new). The logic analyzer data retrieving circuit as claimed in claim 26, wherein counting value of said second counter is stored in said memory unit when said second counter stops counting and then displaying the value on a display screen.

28(new). The logic analyzer data retrieving circuit as claimed in claim 26, further comprising a trigger assembly logic circuit capable of receiving multiple test signals from multiple test samples.

29(new). A logic analyzer data retrieving circuit comprising:

a control unit, comprising a memory and a second counter, adopted for capturing test data from a test sample electrically connected to the logic analyzer data retrieving circuit; and

a time delay circuit, comprising a first counter and a buffer, wherein said buffer is adopted for storing a time delay default value;

wherein at least a clock qualifier signal is preset in said logic analyzer data retrieving circuit based on a specific parameter,

wherein a preset of said first counter is triggered and said default value is transferred from said buffer to said first counter to drive said first counter to start counting in response to said clock qualifier signal until said delay default value is reached and test data from said test sample is continuously captured until said first counter counting teaches said delay default value,

wherein a preset of said second counter is triggered when said first counter counting reaches said delay default value and starts counting until the preset of the first counter is triggered again, and

wherein counting value of aid second counter is stored in said memory unit when said second counter stops counting and then displaying the value on a display screen.

30(new). The logic analyzer data retrieving circuit as claimed in claim 29, wherein counting value of said second counter is stored in said memory unit when said second counter stops counting and then displaying the value on a display screen.

31(new). The logic analyzer data retrieving circuit as claimed in claim 29, further comprising a trigger assembly logic circuit capable of receiving multiple test signals from multiple test samples.